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TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371	ATTORNEY'S DOCKET NUMBER	CE50036P
	U.S. APPLICATION NO. (If known) 10/009509	
INTERNATIONAL APPLICATION NO. PCT/EP00/05148	INTERNATIONAL FILING DATE 1 JUNE 2000	PRIORITY DATE CLAIMED 1 JUNE 1999
TITLE OF INVENTION: COMPLEX MULTIPLIER		
APPLICANT(S) FOR DO/EO/US: HIETALA, ALEX ET AL.		

Applicant herewith submits to the International Bureau of WIPO the following items and other information:

1. ☐ This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☐ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☒ is attached hereto (required only if not communicated by the International Bureau).
   b. ☐ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371 (c)(2)).
   a. ☒ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3)).
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☐ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 – 1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☐ Other items or information.

U.S.AP 10/009509	INTERNATIONAL APPLICATION NO. PCT/EP00/05148	ATTORNEY'S DOCKET NO. CE50036P

21. ☒ The following fees are submitted:

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) – (5)):
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1040.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO $890.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO $740.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) $710.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00

ENTER APPROPRIATE BASIC FEE AMOUNT =				$ 890.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).				$	
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	$	
Total Claims	12 - 20 =		x $18.00	$	
Independent Claims	4 - 3 =	1	x $84.00	$ 84.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+$280.00	$	
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☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by ½.				$	
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Fee for recording the enclosed assignment (37 CFR 1.21 (h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +				$ 40.00	
			TOTAL FEES ENCLOSED =	$	
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a. ☐ A check in the amount of $———— to cover the above fees in enclosed.

b. ☒ Please charge my Deposit Account No. 13-4768 in the amount of **$ 1,014.00** to cover the above fees. A duplicate copy of this sheet is enclosed.

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NOTE: where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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REGISTRATION NUMBER

10/009509
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COMPLEX MULTIPLIER

Field of the Invention

The present invention relates to a complex multiplier, and in particular to a radio receiver incorporating such a complex multiplier, for use in a portable communications device, in which the radio signal to be received is directly down converted to a complex Very Low Intermediate Frequency (VLIF) signal, having In-phase (I) and Quadrature-phase (Q) components, centred around an Intermediate Frequency (IF) which is of the same order of magnitude as the bandwidth of the signal to be received.

Background of the Invention

Most conventional radio receivers for use in portable communication devices such as cellular telephones, are of the super-heterodyne type in which a radio signal to be received is first down-converted to an intermediate frequency (which is still in the radio-frequency (rf) range) and then further down-converted to a base-band signal (having both I and Q components) from which the information contained in the signal may be recovered. Such a receiver is robust. However, direct conversion receivers and, more recently, very low IF receivers have been proposed in order to reduce costs by eliminating both a relatively high performance, and therefore expensive, Surface Acoustic Wave (SAW) or crystal (in the case of AMPS, NADC or other narrow-band systems) band-pass filter (for allowing the wanted IF signal to pass while blocking all unwanted IF signals in neighbouring channels) and one of the two rf local oscillators required in super-heterodyne receivers.

Direct conversion receivers immediately down convert the received radio signal to a base-band signal thus completely eliminating the IF stage. However, such receivers suffer from the formation of a very large unwanted dc component interfering with the base-band signal. This dc component is formed largely by leakage from the local oscillator being received at the

receiver aerial together with the wanted signal, as well as offsets of amplifiers and mixers contained in the receivers.

In order to overcome this problem, a very low IF receiver has been proposed in which the received signal is first down-converted to be centred about an IF which is equal to half the channel spacing (i.e. half the bandwidth of the wanted signal), and then it is down-converted again to base-band. In this way, the dc component which is still formed when the first down-conversion takes place, is located (in frequency) at the very edge of the wanted signal. From here, the unwanted dc component should be able to be relatively easily removed by suitable filtering of the dc component, without losing (very much) information contained in the wanted signal because of the dc component's location at the very edge of the wanted signal.

However, a problem with such an arrangement is that image signals from adjacent and even alternate channels can appear at base-band as unwanted noise interfering with the wanted signal. Such image signals result from imbalances in the analogue components of the I and Q paths between the first down-conversion and the analogue to digital conversion of the I and Q signals.

Summary of the Invention

According to a first aspect of the present invention, there is provided a complex multiplier for multiplying together a first input complex signal, having an In-phase, I, component and a Quadrature-phase, Q, component, and a second input complex signal and generating an output complex signal which is the product of the first and second input signals, the complex multiplier including a gain adjustment multiplier for adjusting the gain of one of the first signal's I and Q components relative to the other and a phase adjustment adder for adjusting the phase of one of the first signal's I and Q components relative to the other.

Preferably, the complex multiplier is a digital complex multiplier and the first and second input signals and the output signal are all digital signals having an associated sampling frequency, f_s.

Preferably, the complex multiplier (which from hereon may be referred to either as a complex multiplier, or as a complex balanced multiplier because of its ability to balance the I and Q components of the first input signal so as to have matching gains and phases) incorporates a quadrature phase generator for receiving a VLIF signal indicative of a Very Low Intermediate Frequency, VLIF, by which the first input complex signal, after relative gain and phase adjustment, is to be down-converted, the quadrature phase generator being adapted to generate the second input complex signal from the VLIF signal. Furthermore, the quadrature phase generator also preferably includes the phase adjustment adder, wherein the phase adjustment adder acts to adjust the phase of one or more of the components of the second input signal.

The VLIF signal may be a real (as opposed to complex) signal communicated to the quadrature phase generator from an external component (such as a controlling digital signal processor, or a VLIF local oscillator), or alternatively, the VLIF signal may be internally generated by the quadrature phase generator itself (e.g. from an internal memory or an internal oscillator, etc.).

In one embodiment, the complex balanced multiplier has a second or higher order gain adjustment multiplier and a second or higher order phase adjustment adder. Preferably, the complex balanced multiplier incorporates an adder arrangement which may be switched between an adding mode and an accumulating mode and which may operate at clocking speeds greater than the sampling frequency of the first input signal, whereby second and higher order terms of each complex multiplication may be calculated and accumulated to first order terms during a single sampling period of the first input signal without requiring additional multipliers.

According to a second aspect of the present invention, there is provided a radio receiver comprising an rf mixer stage for receiving a wanted rf signal and down-converting it to a wanted complex VLIF signal centred around an Intermediate Frequency (IF) which is of the same order of magnitude as the bandwidth of the wanted signal, an analogue to digital converter for converting the complex VLIF signal into a digital complex VLIF signal, and a complex multiplier as set out above for down-converting the digital complex VLIF signal to base-band.

Preferably, the VLIF about which the wanted signal is centred is between 10 and 20 per cent larger than half the channel spacing. Such a choice of IF is particularly advantageous for complex modulation schemes in which each symbol represents two or more bits, as will be required for the evolving standard known as EDGE (Enhanced Data-rate GSM Evolution), and corresponding standards in the US, as with these modulation schemes, it has been surprisingly discovered by the present inventors that significant information is contained in the edge portions of the signal (i.e. up to plus and minus half the channel spacing from the centre of the signal), the loss of which can give rise to an unacceptably large bit or block error rate. An example of a complex modulation scheme in which significant information is contained at the very edge of the channel is 8QPSK (8-position Quadrature Phase Shift Keying) where each symbol represents 3 bits. The term channel spacing, as will be well understood by a person skilled in the art, refers to the separation in terms of frequency between corresponding points in adjacent channels. For example, in GSM the channel separation is 200KHz.

Preferably, the VLIF signal is generated by a local oscillator which may advantageously be a fractional-N phase locked loop (fracNpll). Preferably, the fracNpll is a multi-accumulator fracNpll.

The complex multiplier according to the present invention is advantageous because it permits a difficulty associated with using a VLIF which is larger than half the channel spacing to be overcome. The difficulty is that as you increase the VLIF, you have to increase the band-width of the analogue to

digital converter (adc) and this in turn increases the amount of the negative alternate channel which is admitted by the adc and also increases the amount of this channel which, as an image, appears in the bandwidth of the wanted signal and which must be removed. By providing first or even second-order phase and gain adjustment means, it is possible to set the image rejection to zero (i.e. such that the amount of image components appearing in the base-band signal as noise after passing through the complex multiplier is substantially zero) for one (in the case of first order adjustment means) or even two or more (in the case of second or higher order adjustment means) specific frequencies. In this way, judicious setting of the adjustment means can minimise the effects of the negative alternate channel (which in many systems may in fact be much larger than either adjacent channel).

Setting of the adjustment means to provide for complete image rejection at a certain frequency or frequencies, hereafter referred to as calibration, can be done as a factory adjustment, or, where there is sufficient processing power available to the radio receiver, it could be done automatically by the radio receiver during detection of a known signal (e.g. a mid-amble), or a combination of both techniques could be used whereby an initial factory calibration is performed and then a processor associated with the radio receiver periodically checks the calibration and adjusts it if necessary. Preferably, the calibration is performed separately for a number of different ranges of operation of the radio receiver. For example, setting of the gain adjustment multiplier may be performed for a number of different levels of Automatic Gain Control (AGC) and setting of the phase adjustment adder may be performed for a number of different channels or ranges of channels.

Preferably, the adc takes the form of an over-sampled sigma-delta adc.

Preferably, the radio receiver is formed on an integrated circuit which advantageously includes transmission circuitry for transmitting signals. Ideally, the radio receiver and the transmission circuitry share a number of components such as the local oscillator.

Brief Description of the Drawings

In order that the present invention may be better understood, an embodiment thereof will now be described by way of example only, with reference to the accompanying drawings in which:-

Figure 1 is a block diagram of a radio receiver in accordance with the present invention;

Figure 2 is a diagram illustrating the signal processing performed by the radio receiver of Figure 1 using a wanted GMSK signal and a single negative adjacent channel GMSK signal as an example input to the receiver;

Figure 3 is a diagram illustrating the signal processing performed by the radio receiver of Figure 1 using a wanted GMSK signal and a single negative alternate channel GMSK signal as an example input to the receiver;

Figure 4 is a block diagram of a first order complex balanced multiplier suitable for use in the receiver of Figure 1; and

Figure 5 is a block diagram similar to Figure 4 showing an alternative complex balanced multiplier suitable for use in the receiver of Figure 1.

Detailed Description of the Drawings

Referring to Figure 1, there is shown a Digital Very Low Intermediate Frequency (DVLIF) receiver 1 comprising a Radio Frequency (RF) portion 10, a Very Low Intermediate Frequency (VLIF) portion 30, and a base-band portion 60, with an RF mixer stage 20 located between the RF portion 10 and the VLIF portion 30, and a digital VLIF mixer stage 50 located between the VLIF portion 30 and the base-band portion 60. RF portion 10 comprises an aerial 12, an RF band-pass receive filter 14 and an amplifier 16. RF mixer

stage 20 comprises an In-phase (I) RF mixer 22, a Quadrature-phase (Q) RF mixer 24, a 90° RF phase shifter 26 and an RF Local Oscillator (LO) 28. VLIF portion 30 comprises I and Q IF amplifiers 31,32, I and Q low-pass anti-aliasing filters 33,34 I and Q sigma-delta modulators 35,36, and I and Q digital low pass filters 37,38. Digital VLIF mixer stage 50 comprises a complex balanced multiplier 51 operating as a digital IF mixer, and an IF LO 52. Base-band portion 60 is shown only comprising low pass I and Q digital selectivity filters 61 and 62, though it will of course further comprise the digital processing elements for decoding the digital signals, etc. as will be understood by a person skilled in the art.

The basic operation of the receiver of Figure 1 will now be described. The aerial 12 essentially captures all radio signals which impinge on it and these are fed to the receive filter 14 which attempts to filter away all signals which are outside the frequency range of interest. For example, if the receiver is intended for use as a GSM receiver, the receive filter 14 will greatly reduce the magnitude of all radio signals received by the aerial which are not within the GSM frequency range of 900MHz plus or minus 10% or so. The output from receive filter 14 is then amplified by amplifier 16 before being input to the RF mixing stage 20.

At the RF mixing stage 20, the signals output from the amplifier 16 are down-converted to a VLIF. RF LO 28 generates an RF signal whose frequency is such that the difference between it and the central frequency of the channel which the receiver is trying to receive is equal to the predetermined desired VLIF. The purpose of the 90° phase shifter 26 is to enable I and Q components of the down-converted signals to be output from the I and Q RF mixers 22,24. By generating I and Q components of the signal output by the amplifier 16, it becomes possible to consider the signal as a complex signal having real and imaginary components (corresponding to its I and Q components) and in this way it is possible to distinguish between signals having negative and positive frequencies respectively.

The I and Q signals output by the I and Q RF mixers 22,24 respectively are input to I and Q amplifiers 31,32 and I and Q low pass anti-aliasing filters 33,34 respectively. The purpose of these components is to remove all frequency components of signals arriving at the aerial 12 which are too high (when down-converted) to belong to the signal of interest (which when down-converted will lie approximately between dc and the channel spacing). In practice, because the filters 33,34 are simple (i.e. non-complex), they will also pass the signal contained in the negative adjacent channel (this is the channel located adjacent to the wanted channel substantially on the other side of the frequency of the RF signal generated by the RF LO 28). Furthermore, because real (i.e. non-ideal) filters do not have infinitely sharp cut-off points, the filters 33,34 (to avoid distorting the wanted signal) will also allow a substantial part of both the positive adjacent channel (the channel located adjacent to the wanted channel on the same side of the frequency of the RF signal generated by the RF LO 28 as the wanted channel) and the negative alternate channel (the channel located next but one to the wanted channel on the other side of the frequency generated by the RF LO 28, i.e. the channel adjacent to the negative adjacent channel referred to above).

The signals output from the filters 33,34 are then input to the I and Q sigma-delta modulators 35,36. The sigma-delta modulators 35,36, as will be well understood by a person skilled in the art, generate digital signals which correspond to the input analogue signals plus a large amount of high frequency noise. The digital signals output by the sigma-delta modulators 35,36 are therefore passed through digital low pass filters 37,38 whose purpose is to remove most of the high frequency noise generated by the sigma-delta modulators 35,36 so as to be left with a digital representation of the analog signals passed by the anti-aliasing low-pass filters 33,34 (i.e. the wanted channel, the negative adjacent channel and parts of the positive adjacent channel and the negative alternate channel).

These signals are than input to the digital VLIF mixer stage 50. The primary function of this stage is to further down-convert the wanted signal to base-band (i.e. centred about d.c. frequency). However, in the present invention, it

also performs the function of IQ balancing. IQ balancing means compensating the signals for variations in amplitude and phase between the I and Q components of the signals travelling through the analogue sections of the RF mixing stage 20 and the VLIF portion 30 which are introduced because of differences in the analogue components (or, more precisely, in the responses of the analogue components to the signals passing through them) in the I (22,31,33,35) and Q (24,32,34,36) paths respectively. If these imbalances are not compensated, it results in unwanted image components of signals other than the wanted signal appearing as noise in the same base-band channel as the wanted signal. The way in which this occurs is discussed in greater detail below. Note that the digital VLIF mixer stage 50 is shown as comprising a complex balanced multiplier 51 and an IF LO 52. The complete VLIF mixer stage 50 includes elements for providing the IQ balancing and these are considered as forming part of the complex balanced multiplier as opposed to the IF LO for the purposes of this invention though the exact choice of which component to associate them with is a little arbitrary as will be seen below. Furthermore, although the embodiments described in detail below show a hardware type implementation of complex balanced multipliers, it will be apparent to a person skilled in the art that a sufficiently powerful (in terms of Millions of Instructions Per Second (MIPS)) suitably programmed digital signal processor or microcontroller having a non-specific arithmetic and logic unit and memory. This will be discussed in greater detail below with reference to Figures 4 and 5.

The signals output from the digital VLIF mixer stage 50 are input to the I and Q digital low-pass selectivity filters 61,62 whose purpose is to remove all noise components outside the channel containing the wanted signal. The output from these filters will then typically be fed to a digital signal processor adapted to perform digital signal processing on the I and Q signals output by filters 61,62, such as equalisation, voice decoding etc.

Referring to Figure 2, an example of the signal response of the receiver of Figure 1 will now be described. The first frequency spectrum diagram of Figure 2 shows a wanted signal 100 and a negative adjacent signal 99

centred at 900.2 MHz and 900.0 MHz respectively, together with a dotted line representing the single tone signal 110 generated by RF LO 28. These signals represent typical GSM signals, thus each signal 99,100 has a GMSK spectrum and the channel spacing is 200KHz. According to a preferred embodiment of one aspect of the present invention, the frequency of the RF LO signal 110 is chosen such that the wanted signal when down-converted will be centred about a VLIF which is slightly greater than half the channel spacing, and preferably between 1.1-1.2 times half the channel spacing. Thus in Figure 2, the RF LO signal 110 is shown as being at a frequency of 900.085 MHz. This choice of frequency for the RF LO signal 110 results in the wanted signal 100 being centred about a VLIF of 115 KHz when down-converted by the RF mixer stage 50. A particularly preferred choice of the RF LO according to the present invention would be such as to give rise to the wanted signal being centred about a VLIF of 115.051 KHz which corresponds to 13 MHz/24 * 435/2048 as this frequency can be generated by a Multiple ACCumulator FRACtional-N Phase Locked Loop (MACC FRAC-N PLL) frequency synthesiser. Such a frequency synthesiser is known in the art and is described in, for example, US patent No. 5,111,162 ["Digital Frequency Synthesizer having AFC and Modulation Applied to Frequency Divider," Hietala et al.].

The second frequency spectrum diagram (Figure 2B) of Figure 2 shows the signals 100,99 after having been down converted to a VLIF such that the wanted signal 100 is centred about a VLIF of 115 KHz. The negative adjacent signal is also down converted to a VLIF centred about –85 KHz (note that we are considering the signals as complex signals here which is why it is possible to distinguish between a negative and a positive frequency). Also shown in Figure 2B is a substantially d.c. signal 120 which is referred to as the IM2 (second order intermodulation) signal. The IM2 signal is noise which is generated by a combination of leakage from the RF LO being detected by the aerial 12 and re-combining in essence with itself at the RF mixer stage 20, and second order non-linearities in the analogue mixers 22,24. The effect of filters 33,34 is also shown in Figure 2B by the filter response curve 130.

Because filters 33,34 are real filters, their frequency response is symmetrical about d.c. In order to avoid clipping or distorting the wanted signal 100, the corner frequency of the filters is set beyond 215 KHz. This results in substantially all of the negative adjacent channel 99 (which does not extend much beyond -185 KHz) being passed by these filters 33,34.

Figure 2B also shows some image signals 99',100' which can be referred to as the negative adjacent signal image 99' and the wanted signal image 100'. The negative adjacent signal image 99' is centred around +85KHz while the wanted signal image 100' is centred around -115KHz. These image signals result from imbalances between the I and Q paths, which result, in turn, from imbalances in the analogue components (most precisely in the frequency responses of such components) contained in the different I and Q paths.

The final frequency spectrum diagram (Figure 2C) of Figure 2 shows the wanted 100, negative adjacent 99 and IM2 120, and image 99',100' signals having been further down-converted by the digital VLIF mixer stage 50 such that the wanted signal 100 is now at base-band (i.e. centred about d.c.) and is in a digital format. The negative adjacent signal has been further down-converted and is centred at -200 KHz, while the IM2 signal is located at -115 KHz. The fact that the IM2 signal is located 115 KHz away from the centre of the wanted signal is a critical advantage of the receiver according to the present invention as it permits this signal to be filtered out by either a low pass filter or a notch filter without clipping or distorting the wanted signal 100. Figure 2C also shows the image signals 99',100' which have also be down-converted by -115 KHz such that the negative adjacent signal image 99' is now centred about -30 KHz and the wanted signal image 100' is now centred about -230 KHz. The image signals are also shown as having been reduced in magnitude from Figure 2B, as a result of the I,Q balancing of the VLIF mixer stage 50. This I,Q balancing is the second function of the VLIF mixer stage 50. In practice, the I,Q balancing of the VLIF mixer stage 50 can only be performed substantially perfectly at a particular frequency (or at a few distinct frequencies), however, for the sake of clarity and in order to better see where the optimum frequency or frequencies would be, this notchiness effect

of the VLIF mixer stage is not shown in Figures 2c and 3C. Clearly, the wanted signal image 100' is well separated from the wanted signal 100 (which does not extend substantially beyond ±100 KHz), and thus it would not be worthwhile maximising the balancing of the VLIF mixer stage at this frequency, however the negative adjacent channel image 99' is centred about -30 KHz and will appear in the wanted signal as noise, and thus it might be worthwhile maximising the balancing of the VLIF mixer stage at the central frequency of the negative adjacent signal image 99'.

Referring now to Figure 3, a second example of the signal response of the receiver of Figure 1 will now be described, in which wanted signal 100 and a negative alternate signal 98 centred at 900.2 MHz and 899.8 MHz respectively, are shown arriving at aerial 12 (together with a dotted line representing the single tone signal 110 generated by RF LO 28) in place of the wanted 100 and negative adjacent 99 signals. Of course, when operating in a real environment, the wanted signal 100 will be received together with a large number of other signals including both a negative adjacent and a negative alternate signal; however, for the sake of clarity, Figures 2 and 3 consider only one signal, in addition to the wanted signal, at a time.

The negative alternate signal 98 is spaced from the wanted signal 100 by 400 KHz. The negative alternate signal 98 is shown as being much larger than the wanted signal 100 because, according to the GSM Specifications, an alternate channel can contain signals whose total power is up to 41dB greater than that of the wanted signal 100 as a result of re-use provisions of the cellular structure of a GSM network.

From the second frequency spectrum diagram (Figure 3B) of Figure 3, it can be seen that although a large part of the down-converted negative alternate signal 98 will be filtered by the filters 33,34 (whose frequency response is again shown in Figure 3 by the filter response curve 130), the signal power of the remainder of the negative alternate signal 98 which is still passed by the filters 33,34 is none-the-less significantly large. The main reason for this is simply that the negative alternate signal is just so much bigger than the

wanted signal that even after its power is reduced by the action of the filters it will still be significantly large. Furthermore, since these signals are all Gaussian in terms of their signal strength frequency distribution, and since the negative alternate signal is just so large, its components outside its allotted channel (i.e. spreading into the negative adjacent channel) will also represent a significant level of noise which must be taken into account when designing a receiver.

From the third frequency spectrum diagram (Figure 3C) of Figure 3, it can be seen that for a reasonable amount of imbalance between the I and Q paths of the receiver, and without any balancing being performed by the complex balanced multiplier 51, a relatively large portion of the negative alternate signal image 98' appears in the wanted channel after conversion to base-band (note that image signals 98',100' should really have been included in Figure 3B but have been omitted for the sake of clarity). By comparing Figure 3C with Figure 2C, it is apparent that the negative alternate image 98' will potentially present a greater amount of unwanted noise within the wanted channel than the negative adjacent signal image 99' will. Furthermore, it is apparent that the two images peak at different frequencies (Again, the effect of the balancing of the VLIF mixer stage being effective at only one or a few distinct frequencies is not shown in Figure 3C). Thus, the complex balanced multiplier should preferably be able to perform IQ balancing in such a way as to minimise the effect of at least the negative alternate signal image and ideally both the negative alternate and the negative adjacent signal images.

Figure 4 shows a first order complex balanced multiplier 500. The complex balanced multiplier 500 comprises a quadrature phase generator 510; a Q-path gain adjustment means 520; first, second, third and fourth multipliers 531,532,533,534; and first and second adder/subtractors 541,542. Quadrature phase generator 510 receives a VLIF signal in the form of a phase signal Osd from the IF LO 52 and a programmable Q-path phase correction β as inputs, and outputs cos(Osd), sin(Osd), cos(Osd + β) and sin(Osd + β) signals, which are applied to the second inputs of the first, second, third and fourth multipliers 531,532,533,534 respectively; additionally, the first and second multipliers 531,532 have the digital I-path signal Iin

(output from the digital I filter 37 of Figure 1) applied to their first inputs; while the third and fourth multipliers 533,534 have the digital Q-path signal Qin (output from the digital Q filter 38 of Figure 1) applied to their first inputs. The outputs of the first and fourth multipliers 531,534 are applied as inputs to the first adder/subtractor 541 which outputs a digital baseband I signal Iout; while the outputs of the second and third multipliers 532,533 are applied as inputs to the second adder/subtractor 542 which outputs a digital baseband Q signal Qout.

The effect of the complex balanced multiplier 500 is to generate output I and Q signals Iout and Qout from input signals Iin, Qin and Osd, as set out in equation 1 below:-

$$I_{out} + jQ_{out} = \left(I_{in} + jA_d \cdot e^{j\beta} \cdot Q_{in}\right) \cdot e^{+jO_{sd}} \qquad \text{Equation 1}$$

From Equation 1, it can be seen that if Qin differs from what it is supposed to be because of relative imbalances between the I and Q paths by 1/Ad in gain and -β in phase, then the effect of the complex balanced multiplier 500 is to correct the imbalance as desired. Unfortunately, the imbalance between the paths will not be constant over frequency. Thus the complex balanced multiplier 500 of Figure 1 is only able to exactly balance the I and Q paths at a single frequency. In order to fully describe the imbalance between the paths created by the differences in the analogue components contained in these paths, one must consider the imbalances as being caused by a filter having a Finite Impulse Response (FIR) given by Equation 2 below:-

$$H_{imbalance}(z) = \frac{1}{A_{d0}} \cdot e^{-j\beta_0} + \frac{1}{A_{d1}} \cdot e^{-j\beta_1} \cdot z^{-1} + \frac{1}{A_{d2}} \cdot e^{-j\beta_2} \cdot z^{-2} + \ldots \qquad \text{Equation 2}$$

Clearly, to counter the effect of such an FIR one needs to provide a filter or equivalent means having the response given by Equation 3 below:-

$$H_{balance}(z) = A_{d0} \cdot e^{+j\beta_0} + A_{d1} \cdot e^{+j\beta_1} \cdot z^{-1} + A_{d2} \cdot e^{-j\beta_2} \cdot z^{-2} + \ldots \qquad \text{Equation 3}$$

From equation 3, it is apparent that the first-order compensation provided by complex balanced multiplier 500 corresponds to the first term of $H_{balance}$. In order to provide higher-order compensation or balancing, one could provide a dedicated digital filter having an FIR to compensate for the imbalance up to as many orders as desired. However, it is preferable to re-use some of the elements of the complex multiplier contained within the digital VLIF mixer stage 50.

Figure 5 illustrates a complex balanced multiplier 600 in which some parts are re-used to enable a higher-than-first-order FIR to be performed which can compensate for the imbalance between the I and Q paths at more than one frequency (note that generally speaking, a second order FIR will be able to compensate the imbalance at 2 specific frequencies exactly, while a third order FIR can compensate at 3 specific frequencies, etc.). Specifically, Figure 5 illustrates a fourth order complex balanced multiplier, however, it will be readily apparent to the reader that the arrangement may be modified to alter the order of the FIR of the arrangement, the major constraint being the clock speed available to the re-used elements compared to the sample frequency of the input I and Q signals.

Complex balanced multiplier 600 comprises a Q_{in} storage register 601 and an associated multiplex means 602; a quadrature phase generator 610 and a phase correction β_i storage register 611; a Q-path gain adjustment means 620 and a gain adjustment A_{Di} storage register 621; first, second, third and fourth multipliers 631,632,633,634; first and second adder/subtractors 641,642; I_{out} and Q_{out} storage registers 651,652; and first and second switches 661,662.

The operation of complex balanced multiplier 600 is as follows. The I and Q signals input to the complex balanced multiplier 600 are in the form of digital sampled values. If one considers the sampled values I_{in0}, Q_{in0}, Q_{in-1}, Q_{in-2}, Q_{in-3} where I_{in0} and Q_{in0} are the values of I_{in} and Q_{in} at time t=0, Q_{in-1} is the preceding sampled value of Q_{in} at time $t=-\tau_s$, Q_{in-2} is the value of Q_{in} at time $t=-2\tau_s$, etc., where τ_s is the inverse of the sampling frequency f_s. Q_{in} storage

601 stores the 3 preceding sample values of Q_{in}, namely Q_{in-1}, Q_{in-2}, Q_{in-3}. The associated multiplex means 602 has 4 inputs (namely Q_{in0}, Q_{in-1}, Q_{in-2}, Q_{in-3}) any one of which it can choose to form the output which is passed on to the gain adjustment means 620. Gain adjustment means 620 multiplies together the 2 values appearing at its two inputs, namely the output from multiplex means 602 and the output from the gain adjustment A_{Di} storage register 621 which stores gain adjustment coefficients A_{D0}, A_{D1}, A_{D2}, A_{D3}.

Quadrature phase generator 610 receives as inputs signals Osd and the output from the phase correction β_i storage register 611. The signals output by the quadrature phase generator 610 are cos(Osd) and sin(Osd) which are output at a rate of f_s and cos(Osd + β_i) and sin(Osd + β_i) which are output at a rate of $4f_s$. The signals cos(Osd), sin(Osd), cos(Osd + β) and sin(Osd + β) are applied to the second inputs of the first, second, third and fourth multipliers 631,632,633,634 respectively; additionally, the first and second multipliers 631,632 have the digital I-path signal I_{in0} (output from the digital I filter 37 of Figure 1) applied to their first inputs; while the third and fourth multipliers 633,634 have the output of the gain adjustment means 620 applied to their first inputs. The output of the first multiplier 631 is applied to a first terminal of the first switch 661; the output of the second multiplier 632 is applied to a first terminal of the second switch 662; the output of the third multiplier 633 is applied as an input to the second adder/subtractor 642; and the output of the fourth multiplier 634 is applied as an input to the first adder/subtractor 641. The output of the first adder/subtractor 641 is applied to the I_{out} storage register 651 and the output of the second adder/subtractor 642 is applied to the Q_{out} storage register 652. The output of the I_{out} storage register 651 forms the I_{out} output of the complex balanced multiplier 600 and is additionally fed-back to a second terminal of the first switch 661. The output of the Q_{out} storage register 652 forms the Q_{out} output of the complex balanced multiplier 600 and is additionally fed-back to a second terminal of the second switch 662. First switch 661 acts to connect either its first terminal or its second terminal to an input to the first adder/subtractor 641. Second switch 662 acts to connect either its first terminal or its second terminal to an input of the second adder/subtractor. It will be apparent to the reader that when either

switch 661,662 is connecting the input to the respective adder/subtractor to the second terminal of the switch, that the adder/subtractor together with the respective storage register will act as an accumulator with the running total being stored in the respective storage register.

Consider now that the desired outputs from the complex balanced multiplier 600 are given by equation 4 below:-

$$I_{out} + jQ_{out} = (I_{in0} + jQ_{in0} \cdot A_{D0} \cdot e^{j\beta 0} + jQ_{in-1} \cdot A_{D1} \cdot e^{j\beta 1} + ... + jQ_{in-3} \cdot A_{D3} \cdot e^{j\beta 3})e^{jOsd}$$

(Equation 4)

In order to achieve the I_{out} and Q_{out} signals given by this equation, the complex balanced multiplier operates four cycles in every sampling period τ_s. In the first cycle, the terms $I_{in0}*e^{jOsd}$ and $jQ_{in0}*A_{D0}*e^{j\beta 0}*e^{jOsd}$ are calculated. To do this, multilplex means 602 selects its first input which receives Q_{in0} as its output and gain adjustment storage register 621 outputs gain adjustment constant A_{D0} which is then multiplied with Q_{in0} at the gain adjustment means 620 to generate $Q_{in0}*A_{D0}$. Also phase adjustment storage register 611 outputs β_0 which is used by the quadrature phase generator 610 to generate the real (cos) and imaginary (sin) components of e^{jOsd} and $e^{j(\beta 0+Osd)}$ respectively. These components are appropriately multiplied with I_{in0} and Q_{in0} in multipliers 631 to 634 and the real and imaginary terms are appropriately added together in adder/subtractors 641 and 642 to produce the real and imaginary parts of $(I_{in0}+jQ_{in0}*A_{D0}*e^{j\beta 0})*e^{jOsd}$ respectively. These are then stored in the I_{out} and Q_{out} storage registers 651,652 respectively and the first cycle comes to an end.

During the second cycle, first and second switches 661,662 are switched into their second state such that the output of the storage registers 651,652 are fed back to the first inputs of the adder/subtractors 641,642. Also, multiplex means 602 selects its second input which receives Q_{in-1} from Q_{in} storage register 601 as its output; gain adjustment storage register 621 outputs A_{D1} to gain adjustment means 620; and phase adjustment means 611 outputs β_1 to

the quadrature phase generator 610 which generates real and imaginary components of $e^{j(\beta 1+Osd)}$ which are multiplied with the output of gain adjustment means 620 (i.e. $Q_{in-1}*A_{D1}$) in multipliers 633 and 634 to generate imaginary and real components of the term $jQ_{in-1}*A_{D1}* e^{j(\beta 1+Osd)}$ which are accumulated to the values stored in storage registers 652 and 651 respectively; the new totals are then restored in registers 652 and 651 ready for the third and fourth cycles.

The third and fourth cycles proceed in an analogous way to the second cycle until all of the components required by Equation 4 have been calculated whereupon signals I_{out} and Q_{out} become valid; switches 661 and 662 are returned to their first positions; and new sample values of I_{in}, Q_{in} and Osd are received at the inputs to the complex balanced multiplier 600.

It will by now be apparent to the reader that the present invention provides a complex balanced multiplier which permits a radio receiver architecture which has all of the advantages of a direct conversion receiver in terms of the lack of an expensive SAW filter and a second rf local oscillator, and which is none-the-less able to receive narrow-band (e.g. 200KHz) radio-signals having greater than first order modulation (i.e. 2 or more bits per symbol) transmitting symbols at rates of the order of 20-30 thousand symbols per second (in which the adjacent and alternate channels may contain noise having a significantly greater magnitude than the magnitude of the wanted signal, in accordance with GSM specifications or similar). The complex balanced multiplier permits the use of a local oscillator which down-converts the wanted signal to a VLIF centred about a frequency which is between 1.1 and 1.2 times half the channel spacing. The use of a complex balanced multiplier according to the present invention to perform the VLIF to base-band down-conversion minimises the additional amount of noise placed into the wanted signal channel at base-band from the negative alternate image channel as a result of this choice of VLIF. Optimally, a second or higher order balanced complex multiplier is used which permits substantially perfect image rejection at two or more frequencies which may be pre-programmed to minimise the effects of noise from unwanted image signals.

The complex balanced multipliers of Figures 4 and 5 are examples of possible implementations only and alternative implementations will be readily apparent to persons skilled in the art. For example, instead of using a serial implementation to generate a greater than first order adjustment means, one could use a parallel implementation in which more real multipliers are used to generate the higher order terms in parallel with the first order terms. Alternatively, one could simply employ a non-specific digital signal processor (dsp) or microcontroller suitably programmed to perform the desired complex multiplications with the relevant IQ balancing operations incorporated therein. Obviously, for applications such as GSM or EDGE a very powerful digital signal processor (in terms of its MIPS, relative to today's standards) would be required which would make it an unattractive solution at present but obviously if dsp's continue to become cheaper and more powerful it may be a viable solution in the future.

CLAIMS

1. A complex multiplier for multiplying together a first input complex signal, having an In-phase, I, component and a Quadrature-phase, Q, component, and a second input complex signal and generating an output complex signal which is the product of the first and second input signals, the complex multiplier including a gain adjustment multiplier for adjusting the gain of one of the first signal's I and Q components relative to the other and a phase adjustment adder for adjusting the phase of one of the first signal's I and Q components relative to the other, wherein the gain adjustment multiplier is a second or higher order gain adjustment multiplier and the phase adjustment adder is a second or higher order phase adjustment adder..

2. A complex multiplier as claimed in claim 1 wherein the complex multiplier is a digital complex multiplier and the first and second input signals and the output signal are all digital signals having an associated sampling frequency, f_s.

3. A complex multiplier as claimed in either one of the preceding claims including a quadrature phase generator for receiving a VLIF signal indicative of a Very Low Intermediate Frequency, VLIF, by which the first input complex signal, after relative gain and phase adjustment, is to be down-converted, the quadrature phase generator being adapted to generate the second input complex signal from the VLIF signal.

4. A complex multiplier as claimed in claim 3 wherein the quadrature phase generator includes the phase adjustment adder, wherein the phase adjustment adder acts to adjust the phase of one or more of the components of the second input signal, to thereby adjust the phase of one of the I and Q components of the first input signal.

5. A complex multiplier as claimed in any one of the preceding claims further comprising an adder arrangement which may be switched between an adding mode and an accumulating mode and which may operate at clocking

speeds greater than the sampling frequency of the first input signal, whereby second and higher order terms of each complex multiplication may be calculated and accumulated to first order terms during a single sampling period of the first input signal without requiring additional multipliers

6. A radio receiver comprising an rf mixer stage for receiving a wanted rf signal and down-converting it to a wanted complex VLIF signal centred around an Intermediate Frequency (IF) which is of the same order of magnitude as the bandwidth of the wanted signal, an analogue to digital converter for converting the complex VLIF signal into a digital complex VLIF signal, and a complex multiplier as claimed in any one of the preceding claims for down-converting the digital complex VLIF signal to base-band.

7. A radio receiver as claimed in claim 6 wherein the gain adjustment multiplier and the phase adjustment adder, of the complex multiplier as claimed in any one of claims 1-5, are adapted to provide close to perfect balancing at a frequency close to an edge of the base-band frequency spectrum whereby the amount of the image signal from the negative alternate channel is minimised.

8. A radio receiver as claimed in either one of claims 6 or 7 wherein the IF about which the wanted VLIF signal is centred is between 10 and 20 per cent larger than half the channel spacing.

9. A radio receiver as claimed in any one of claims 6, 7 or 8 wherein the local oscillator is a fractional-N phase locked loop frequency synthesiser.

10. A radio receiver as claimed in claim 9 wherein the fractional-N phase locked loop frequency synthesiser incorporates two or more accumulators.

11. A radio receiver as claimed in any one of claims 7 to 10 wherein the analogue to digital converter takes the form of an over-sampled sigma delta analogue to digital converter.

12. A radio receiver as claimed in any one of claims 7 to 11 formed as an integrated circuit.

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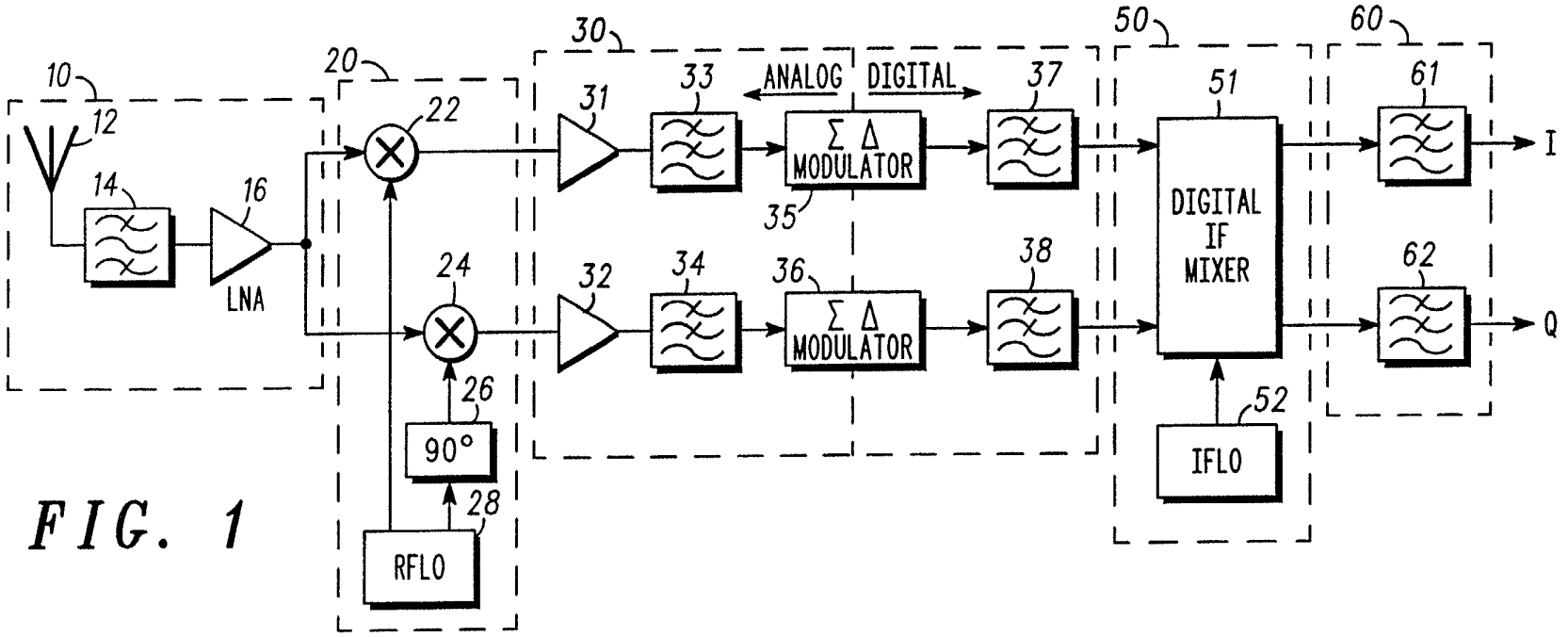

FIG. 1

FIG. 2

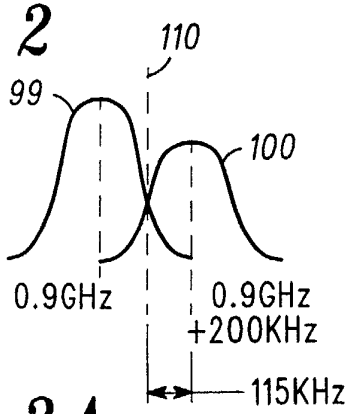

FIG. 2A

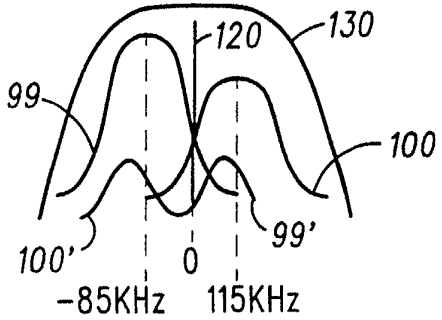

FIG. 2B

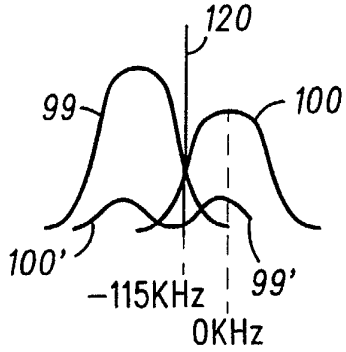

FIG. 2C

10/009509

FIG. 3

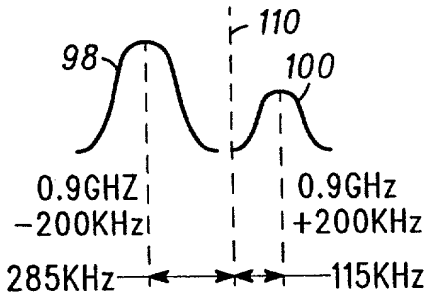

FIG. 3A

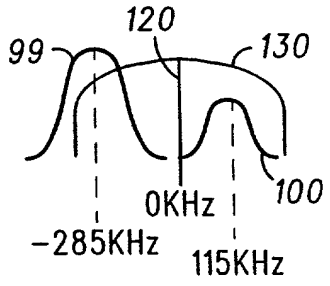

FIG. 3B

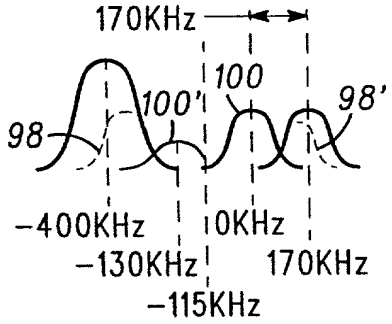

FIG. 3C

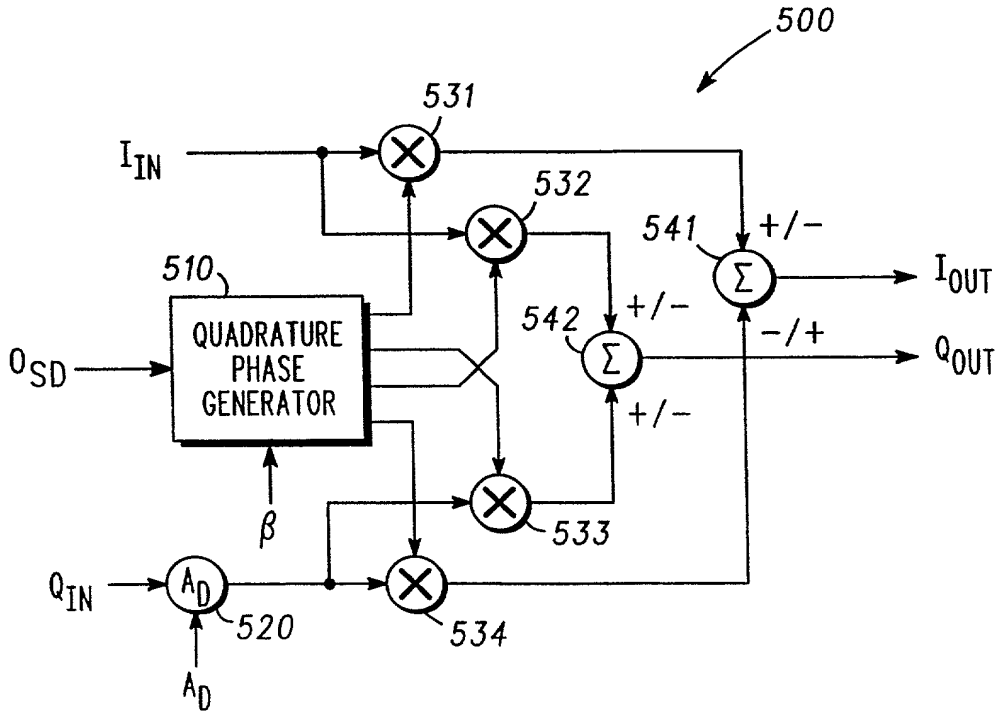

FIG. 4

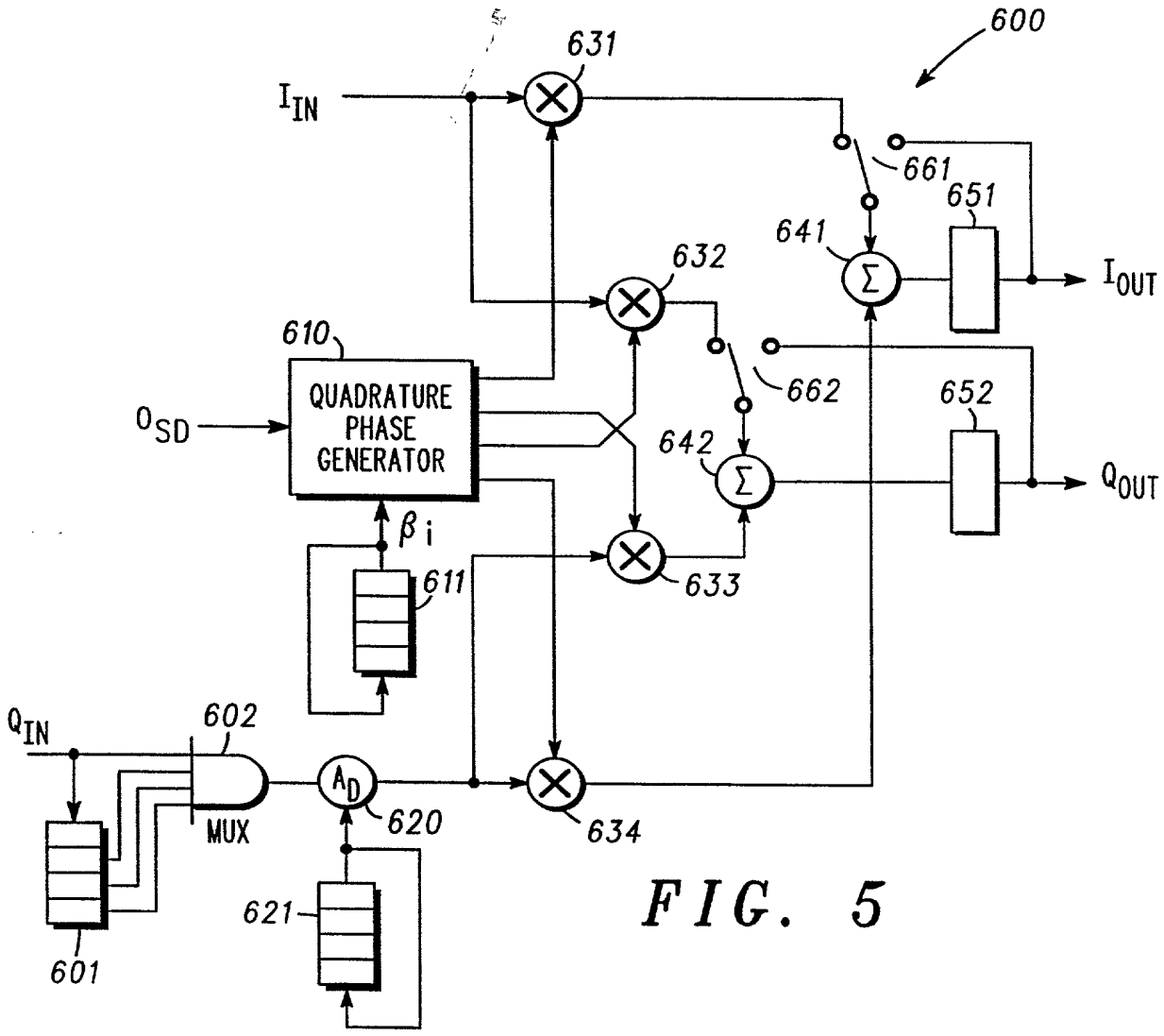
600
631
I_{IN}
661
651
641
632
I_{OUT}
610
QUADRATURE PHASE GENERATOR
O_{SD}
662
652
642
Q_{OUT}
β i
611
633
Q_{IN}
602
A_D
620
MUX
634
621
601

FIG. 5

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

Attorney Docket CE50036P

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below), or an original, first and joint inventor (if plural names are listed below), of the subject matter which is claimed and for which a patent is sought on the invention entitled COMPLEX MULTIPLIER, the specification of which is attached hereto unless the following box is checked:

☑ Application was filed on 01 JUNE 2000
as Application No. PCT/EP00/05148
and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed
99401319.1	EPC	1 JUNE 1999	☑ Yes ☐ No
(Number)	(Country)	(Day/Month/Year Filed)	
_____	_____	_____	☐ Yes ☐ No
(Number)	(Country)	(Day/Month/Year Filed)	

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal

Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)
(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Jonathan P. Meyer, Reg. No. 30,477; Doug Fekete, Reg. No. 29,065; K. Cyrus Khosravi, Reg. No. 40,375; Steven G Parmelee, Reg. No. 28,790; J. Ray Wood, Reg. No. 36,062; Daniel K. Nichols, Reg. No. 29,420; Val Jean Hillman, Reg. No. 34,841; Susan L. Lukasik, Reg. No. 35,261; Terri S. Hughes, Reg. No. 41,856; Steven R. Santema, Reg. No. 40,156.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)
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Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)
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		20 Oct 01

3-00

3-01

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Same as above		

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